

Description

[THIN FILM TRANSISTOR MANUFACTURE METHOD]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of a prior application serial no. 10/248,521, filed January 27, 2003, which claims the priority benefit of Taiwanese application serial no. 91111642, filed on May 31, 2002.

BACKGROUND OF INVENTION

[0002] Field of Invention

[0003] The present invention generally relates to a Thin Film Transistor (TFT) manufacture method, and more particularly, to a manufacture method of making an a-Si layer in the TFT. The method optimizes the electric characteristics of the TFT, and restrains the photo-leakage current generated when the a-Si layer in the TFT is irradiated by the light.

[0004] Description of Related Art

[0005] The fast growth of multimedia has mainly benefited from the great improvement in semiconductors and display apparatus. For the display, the Cathode Ray Tube (CRT) has continuously monopolized the display market in recent years due to its excellent display quality and advantage of being cost-effective. However, for the environment of the user using multiple terminals/display apparatus on a desktop, or from the environmental protection viewpoint and the trend of saving energy, CRTs have many problems due to deficiencies of space utilization and power consumption. As a result, CRTs cannot fulfill the requirements of the lighter, thinner, shorter, and smaller as well as low power consumption. Therefore, the Thin Film Transistor Liquid Crystal Display (TFT-LCD) having the advantages of the high display quality, good space utilization, low power consumption, and no radiation gradually has become the mainstream.

[0006] The general TFT-LCD mainly constitutes an LCD panel and a driving circuit. Wherein, the LCD panel comprises a TFT array substrate, a color filter substrate (C/F substrate), and a liquid crystal layer located in between these two substrates. The photo film plates such as the polarizer, the photo-intensity plate, and the diffusion plate are at-

tached to the outside of two substrates. The driving circuit is generally bonded to the panel with the chip-bond manner. The Chip On Board (COB), the Chip On Glass (COG), and the Tape Automated Bonding (TAB) manners are generally used. Moreover, since the liquid crystal molecule cannot emit light itself, the light source with enough intensity must be provided for LCD to perform the display operation. For the reflection type panel, the light source generally comes from a front light module or an external light source. For the penetration type panel, the light source generally comes from a back light module.

[0007] The well known TFT can be generally divided into two different types: the a-Si layer TFT and the polycrystalline silicon TFT. Since the manufacture process of the a-Si TFT is simpler compared to the manufacture process of the polycrystalline silicon TFT, the technique of liquid crystal driven by the a-Si TFT array is still mainstream. However, there are some problems that exist in the a-Si TFT element itself, for example, the a-Si layer in the TFT will generate the photo leakage current I_{photo} after it is irradiated by the front light source, the back light source or the external light source. The photo leakage current I_{photo} not only impacts the performance of the TFT element itself,

but also generates problems such as frame flicker or cross talk when the frame is displayed.

[0008] FIG. 1 schematically shows a flow chart for making the a-Si layer (channel layer) in a conventional TFT. Referring to FIG. 1, the a-Si layer (channel layer) in the conventional TFT is generally formed above the gate by using the Chemical Vapor Deposition (CVD) method. The manufacture of the a-Si layer is generally performed in three phases: (1) forming a first a-Si layer with a low deposition rate (LDR); (2) forming a second a-Si layer with a high deposition rate (HDR); and (3) performing the N+Mixed to the second a-Si layer to form a N+Mixed a-Si layer.

[0009] FIG. 2 lists the manufacture process parameters used in the first a-Si layer formed by using the LDR and the second a-Si layer formed by using the HDR in the prior art. Referring to FIG. 2, when the first a-Si layer is formed by using the LDR, the flux of SiH_4 is 4400 sccm, the flux of H_2 is 22000 sccm, and the flux ratio of H_2/SiH_4 is 5.0. Moreover, the operating pressure used to form the film of the first a-Si layer film is 1.1 mbar, and the power of the radio frequency (RF) is 140W. Such a high flux of H_2 can achieve the objective of repairing the defects. It means a large amount of the H_2 links with the dangling bonds in the first

a-Si layer, so that the number of the defects in the first a-Si layer can be reduced. In other words, the first a-Si layer with high quality film can be formed by controlling the H_2/SiH_4 flux ratio to stay at about 5.0 to perform the film forming with LDR.

- [0010] Similarly, referring to FIG. 2, after the first a-Si layer is formed, the second a-Si layer is formed above the first a-Si layer by using the HDR. The flux of the SiH_4 is 5700 sccm, the flux of H_2 is 5400 sccm, and the flux ratio of H_2/SiH_4 is 0.95. Moreover, the operating pressure used to form the film of the second a-Si layer film is 1.4 mbar, and the RF power is 250W.
- [0011] FIG. 3 lists the electric characteristics and averages of the conventional TFT. Referring to FIG. 3, the channel layer in the conventional TFT is made by using the manufacture process conditions listed in FIG. 2. The average of the on current I_{on} of the conventional TFT is about $6.572\mu A$, the average of the off current I_{off} is about $4.7278pA$, the average of the threshold voltage V_{th} is about $3.3496V$, and the average of the electronic migration rate μ_{fe} is about $0.5588cm^2/v.s.$
- [0012] The flux ratio of H_2/SiH_4 is controlled to stay at about 5.0 when the first a-Si layer is made by using the LDR in the

prior art. The high flux of H_2 is applied to the first a-Si layer to repair the defects, and further to have the off current I_{off} reduce to about 4.7278pA (below 5pA). However, when evaluating the performance of the a-Si TFT element itself, besides considering the parameters such as the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} , the photo leakage current I_{photo} of the element is also served as a factor of the evaluation. The on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} of the conventional TFT are all in the adequate range. However, the TFT generates photo leakage current I_{photo} after it is irradiated by the front light source, the back light source or the external light source. The photo leakage current I_{photo} generated usually is about 1E-10 Amp, and it significantly deteriorates the display quality.

SUMMARY OF INVENTION

[0013] Therefore, the objective of the present invention is to provide a TFT manufacture method. The method efficiently improves the photo leakage current problem without impacting the electric characteristics such as the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} .

[0014] In order to achieve the objective mentioned above, a TFT manufacture method is provided, comprising the steps of follows. At first, a substrate is provided, and a gate and a gate isolation layer that covers the gate are provided on the substrate. Then, the first a-Si layer is formed by using an LDR, wherein the first a-Si layer is formed under the condition of the flux ratio of H_2/SiH_4 being in the range from 0.40 to 1.00. The second a-Si layer is subsequently formed by using the HDR, wherein the second a-Si layer is formed under the condition of the flux ratio of H_2/SiH_4 being within a range from 0.95 to 1.00. Afterwards, the N+Mixed a-Si layer is formed on the surface of the second a-Si layer. The N+Mixed a-Si layer is formed, for example, by performing an N-type ion implantation on the surface of the second a-Si layer. After the manufacture of the film layer mentioned above is completed, the first a-Si layer, the second a-Si layer, and the N+Mixed a-Si layer are defined to form a channel layer. Finally, a source/drain is formed on both sides of the channel layer to constitute a three electrodes TFT having a gate, a source and a drain.

[0015] In the TFT manufacture method of the present invention, a passivation layer is further formed on the substrate after the source/drain is formed to cover the whole TFT, so as

to further assure the reliability of the TFT element.

- [0016] In the TFT manufacture method of the present invention, the conditions of the manufacture process to form the first a-Si layer are as follows: the flux of the SiH₄ is about 1000 to 4600 sccm, the flux of H₂ is about 400 to 4600 sccm, the operating pressure is about 0.75 to 1.00 mbar, and the RF power is about 70 to 100 W.
- [0017] In the TFT manufacture method of the present invention, the conditions of the manufacture process to form the second a-Si layer are as follows: the flux of the SiH₄ is from about 1000 to 5700 sccm, the flux of H₂ is from about 950 to 5700 sccm, the operating pressure is from about 1.3 to 1.6 mbar, and the RF power is from about 200 to 320 W.
- [0018] In the TFT manufacture method of the present invention, the thickness of the first a-Si layer is between about 100 to 500 angstroms, the thickness of the second a-Si layer is between about 1000 to 2000 angstrom, and the thickness of the N+Mixed a-Si layer is between about 200 to 400 angstrom.
- [0019] In order to achieve the objective mentioned above, an a-Si layer manufacture method is provided, comprising the steps of as follows. At first, a substrate is provided. Then,

a first a-Si layer is formed on the substrate by using the Chemical Vapor Deposition (CVD) method, wherein, the first a-Si layer is formed under the condition of the flux ratio of H_2/SiH_4 being within a range from 0.40 to 1.00. Afterwards, a second a-Si layer is formed above the first a-Si layer by using the CVD method, wherein, the second a-Si layer is formed under the condition of the flux ratio of H_2/SiH_4 being within a range from 0.95 to 1.00.

- [0020] In the a-Si layer manufacture method of the present invention, the conditions of the manufacture process to form the first a-Si layer are as follows: the flux of the SiH_4 is about 1000 to 4600 sccm, the flux of H_2 is about 400 to 4600 sccm, the operating pressure is such as 0.75 to 1.00 mbar, and the RF power is about 70 to 100 W.
- [0021] In the a-Si layer manufacture method of the present invention, the conditions of the manufacture process to form the second a-Si layer are as follows: the flux of the SiH_4 is from about 1000 to 5700 sccm, the flux of H_2 is from about 950 to 5700 sccm, the operating pressure is from about 1.3 to 1.6 mbar, and the RF power is from about 200 to 320 W.
- [0022] In the a-Si layer manufacture method of the present invention, the thickness of the first a-Si layer is between

about 100 to 500 angstrom, and the thickness of the second a-Si layer is between about 1000 to 2000 angstrom.

BRIEF DESCRIPTION OF DRAWINGS

- [0023] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention.
- [0024] FIG. 1 schematically shows a flow chart for making the a-Si layer (channel layer) in a conventional TFT.
- [0025] FIG. 2 lists the manufacture process parameters used in the first a-Si layer formed by using the LDR and the second a-Si layer formed by using the HDR in the prior art.
- [0026] FIG. 3 lists the electric characteristics and averages of the conventional TFT.
- [0027] FIG. 4A-4F schematically shows cross-sections of the TFT manufacture process.
- [0028] FIG. 5 lists the manufacture process parameters used in the first embodiment and the first a-Si layer formed by using the LDR in the prior art.
- [0029] FIG. 6 lists the manufacture process parameters used in the first embodiment and the second a-Si layer formed by

using the HDR in the prior art.

- [0030] FIG. 7–11 respectively lists the electric characteristics and averages of the TFT in the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A).
- [0031] FIG. 12 schematically shows a comparison table of the electric characteristics of the TFT in the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A).
- [0032] FIG. 13–16 respectively shows a comparison table of the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} in the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A) and in the conventional TFT.
- [0033] FIG. 17 schematically shows a comparison table of the electrical characteristics of the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A) and the conventional TFT.
- [0034] FIG. 18 is a table schematically showing the relationship of the thickness of the second a-Si layer in the TFT and its electrical characteristics.
- [0035] FIG. 19–22 respectively shows the impact of the thickness of the second a-Si layer to the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} .

DETAILED DESCRIPTION

[0036] THE FIRST EMBODIMENT

[0037] FIG. 4A-4F schematically shows the sectional sketch maps of the TFT manufacture process. Referring to FIG. 4A first, a substrate 100 is provided, the substrate 100 is a substrate such as glass substrate or substrate made of other transparent materials. A gate 102 is subsequently formed on the substrate 100. The gate 102 is formed via the method of forming the Metal 1 overall on the substrate 100 first, then the Metal 1 mentioned above is defined by using the manufacture process of the microfilm and etch to form the gate 102, wherein the gate 102 is made of conductive materials such as Ta and Cr.

[0038] Then, referring to FIG. 4B, after the gate 102 is formed, a gate isolation layer 104 is formed on the substrate 100. The gate isolation layer 104 covers the gate 102, wherein the gate isolation layer 104 is made of material such as SiN_x , SiO_x , or other dielectric materials.

[0039] Then, referring to FIG. 4C, after the gate isolation layer 104 is formed, a first a-Si layer 106a and a second a-Si layer 106b are formed sequentially, and a N+Mixed a-Si layer 106c is subsequently formed on the surface of the

second a-Si layer 106b. The first a-Si layer 106a is formed by using the CVD with LDR, and the thickness of the first a-Si layer 106a is from 100 to 500 angstroms. The second a-Si layer 106b is formed by using the CVD with HDR, and the thickness of the second a-Si layer 106b is from 1000 to 2000 angstroms. The N+Mixed a-Si layer 106c is formed by using the ion implantation method, and the thickness of the formed N+Mixed a-Si layer is from 200 to 400 angstroms. The manufacture conditions for forming the first a-Si layer 106a and the second a-Si layer 106b are described in detail accompanying FIG. 5 and FIG. 6 hereinafter.

- [0040] Referring to FIG. 4D, after the first a-Si layer 106a, the second a-Si layer 106b, and the N+Mixed a-Si layer 106c are formed, the patterns of the first a-Si layer 106a, the second a-Si layer 106b, and the N+Mixed a-Si layer 106c are defined by using the microfilm and etch method to form the channel layer 106.
- [0041] Referring to FIG. 4E, after the channel layer 106 is formed, a source/drain 108 is formed on both sides of the channel layer 106. The source/drain 108 is formed via the method of forming a Metal 2 overall first, then the Metal 2 mentioned above is defined by using the manufacture process

of the microfilm and etch to form the source/drain 108. The source/drain 108 is made of conductive materials such as Al/Cr and Ti.

[0042] Finally, referring to FIG. 4F, after the source/drain 108 is formed, a passivation layer 110 is further formed on the substrate 100 to cover the three electrodes TFT having the gate 102 and the source/drain 108, so as to further improve the reliability of the elements. Wherein, the passivation layer 110 is made of a material such as SiN_x or polyimide.

[0043] FIG. 5 lists the manufacture process parameters used in the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A) and the first a-Si layer formed by using the LDR in the prior art. Referring to FIG. 5, when the first a-Si layer is formed by using the LDR in the prior art, the flux of the SiH_4 is 4400 sccm, the flux of H_2 is 22000 sccm, the flux ratio of H_2/SiH_4 is 5.0, the operating pressure is 1.1 mbar, and the RF power is 140W. When the first a-Si layer is formed by using the LDR according to the present invention, the flux of the SiH_4 is from 1000 to 4400 sccm, the flux of H_2 is from 400 to 4600 sccm, the flux ratio of H_2/SiH_4 is from 0.40 to 1.00, the operating pressure is from 0.75 to 1.00 mbar, and the RF power is

from 70 to 100W. The major difference between the prior art and the present invention is the flux ratio of H_2/SiH_4 is adjusted from 5.0 to a range from 0.40 to 1.00.

[0044] In the present invention, when the first a-Si layer 106a is formed, the flux ratio of H_2/SiH_4 is intentionally adjusted from the 5.0 used in the prior art to a range from 0.40 to 1.00, so as to reduce the repairing level of the defects in the first a-Si layer by reducing the ratio of the H_2 flux. In other words, the first a-Si layer formed in the present invention has more defects.

[0045] FIG. 6 lists the manufacture process parameters used in the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A) and the second a-Si layer formed by using the HDR in the prior art. Referring to FIG. 6, when the second a-Si layer is formed by using the HDR in the prior art, the flux of the SiH_4 is 5700 sccm, the flux of H_2 is 5400 sccm, the flux ratio of H_2/SiH_4 is 0.95, the operating pressure is 1.4 mbar, and the RF power is 250W. When the second a-Si layer is formed by using the HDR according to the present invention, the flux of the SiH_4 is from 1000 to 5700 sccm, the flux of H_2 is from 950 to 5700 sccm, the flux ratio of H_2/SiH_4 is from 0.95 to 1.00, the operating pressure is from 1.3 to 1.6 mbar, and the RF

power is from 200 to 320W. It is known from the description mentioned above that there is no big difference between the prior art and the present invention in the manufacture process conditions to form the second a-Si layer.

[0046] FIG. 7-11 respectively lists the electric characteristics and averages of the TFT in the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A). Referring to FIG. 7 first, in DB025A, the average of the on current I_{on} is about $7.9112\mu A$, the average of the off current I_{off} is about $3.5382pA$, the average of the threshold voltage V_{th} is about $2.4096V$, and the average of the electronic migration rate μ_{fe} is about $0.61\text{ cm}^2/\text{v.s.}$

[0047] Then, referring to FIG. 8, in DT394A, the average of the on current I_{on} is about $7.8488\mu A$, the average of the off current I_{off} is about $2.6698pA$, the average of the threshold voltage V_{th} is about $2.6919V$, and the average of the electronic migration rate μ_{fe} is about $0.6239\text{ cm}^2/\text{v.s.}$

[0048] Then, referring to FIG. 9, in DT395A, the average of the on current I_{on} is about $8.3186\mu A$, the average of the off current I_{off} is about $2.1618pA$, the average of the threshold voltage V_{th} is about $2.6004V$, and the average of the electronic migration rate μ_{fe} is about $0.6571\text{ cm}^2/\text{v.s.}$

[0049] Then, referring to FIG. 10, in DB340A, the average of the

on current I_{on} is about $8.23975\mu A$, the average of the off current I_{off} is about $2.885625pA$, the average of the threshold voltage V_{th} is about $1.94425V$, and the average of the electronic migration rate μ_{fe} is about $0.605375\text{ cm}^2/\text{v.s.}$

[0050] Then, referring to FIG. 11, in DT293A, the average of the on current I_{on} is about $7.8982\mu A$, the average of the off current I_{off} is about $2.7052pA$, the average of the threshold voltage V_{th} is about $2.2835V$, and the average of the electronic migration rate μ_{fe} is about $0.6009\text{ cm}^2/\text{v.s.}$

[0051] FIG. 12 schematically shows a comparison table of the electric characteristics of the TFT in the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A). Referring to FIG. 12, in five sets of the experiment of the present embodiment, the average of the on current I_{on} is about $8.043314\mu A$, the average of the off current I_{off} is about $2.792125pA$, the average of the threshold voltage V_{th} is about $2.38593V$, and the average of the electronic migration rate μ_{fe} is about $0.61938\text{ cm}^2/\text{v.s.}$

[0052] When the first a-Si layer is made in the present embodiment, since the flux ratio of H_2/SiH_4 is adjusted to stay on a range from 0.40 to 1.00, the formed first a-Si layer has more defects. However, from FIG. 7-11 and FIG. 12 men-

tioned above, compared to the prior art, the impact of the behavior of the defects that exist in the first a-Si layer on the TFT electric characteristics considered as a whole, such as the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} , is still better than in the prior art.

[0053] FIG. 13-16 respectively shows a comparison table of the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} in the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A) and in the conventional TFT. Referring to FIG. 13-16, in five sets of the experiment of the present embodiment, the behavior of the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} performed are all better than in the prior art. It is clear from FIG. 13 that the TFT of the present embodiment has higher on current I_{on} . It is clear from FIG. 14 that the TFT of the present embodiment has lower off current I_{off} . It is clear from FIG. 15 that the TFT of the present embodiment has lower threshold voltage V_{th} . Moreover, it is also clear from FIG. 16 that the TFT of the present embodiment has higher electronic migration rate μ_{fe} .

[0054] FIG. 17 schematically shows a comparison table of the electrical characteristics of the first embodiment (DB025A, DT394A, DT395A, DB340A, and DT293A) and the conventional TFT. Referring to FIG. 17, the on current I_{on} of the TFT in the present embodiment is raised from 6.57 μ A used in the prior art to 8.04 μ A, the off current I_{off} is lowered from 4.72pA used in the prior art to 2.79pA, the threshold voltage V_{th} is lowered from 3.34V used in the prior art to 2.38V, and the electronic migration rate μ_{fe} is raised from 0.55cm²/v.s used in the prior art to 0.62 cm²/v.s.

[0055] Similarly, referring to FIG. 17, the present invention not only improves the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} of the elements, but also improves the photo leakage current phenomenon when the element is irradiated by the light. The TFT photo leakage current I_{photo} of the present embodiment is lowered to 5E-11 from 1E-10 used in the prior art, the element photo leakage current I_{photo} is lowered nearly an order. The reason the photo leakage current I_{photo} can be reduced is that the first a-Si layer formed in the present embodiment has a larger number of defects compared to the prior art, and these defects trap

the photo leakage current in the first a-Si layer, so that the element photo leakage current I_{photo} is reduced.

[0056] However, the TFT manufacture process shown in FIG. 4A-4F is only exemplified for description, and the present invention is not limited to only apply in this manufacture process. The method of the present invention to form the first a-Si layer by reducing the flux ratio of H_2/SiH_4 can be applied in other TFT manufacture process.

[0057] THE SECOND EMBODIMENT

[0058] It is known by those who are skilled in the related art that the film quality and the film thickness of the first a-Si layer, the second a-Si layer and the N+Mixed a-Si layer determine the TFT electrical characteristics such as the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} . The first embodiment of the present invention probed into the manufacture process conditions (the portion of the film quality) for making the first a-Si layer as mentioned above. The present embodiment probes into the relationship between the thickness of the second a-Si layer and the electrical characteristics of the element hereinafter.

[0059] FIG. 18 is a table schematically showing the relationship of the thickness of the second a-Si layer in the TFT and its

electrical characteristics. Referring to FIG. 18, in the present embodiment, the thickness of the first a-Si layer is fixed to stay at about 100 angstroms, the thickness of the N+ Mixed a-Si layer is fixed to stay at about 300 angstroms, and the thickness of the second a-Si layer is fixed to stay at about 1000 angstroms, 1250 angstroms, 1500 angstroms, 1750 angstroms, and 2000 angstroms respectively.

[0060] When the thickness of the second a-Si layer increases from 1000 angstroms to 2000 angstroms, the on current I_{on} is increased from $3.5415\mu A$ to $6.1005\mu A$, the off current I_{off} is reduced from $4.19775pA$ to $3.61125pA$, the threshold voltage V_{th} is reduced from $5.27225V$ to $3.15425V$, and the electronic migration rate μ_{fe} is increased from $0.38675\text{ cm}^2/\text{v.s}$ to $0.5145\text{ cm}^2/\text{v.s}$.

[0061] FIG. 19-22 respectively show the impact of the thickness of the second a-Si layer to the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} . From FIG. 19-21, the on current I_{on} is increased along with the increase of the thickness of the second a-Si layer, and the off current I_{off} stays on about 4pA. However, when the thickness of the second a-Si layer increases to 2000 angstroms, the off current I_{off} is

reduced to about 3.6pA. The threshold voltage V_{th} is reduced along with the increase of the thickness of the second a-Si layer, and the electronic migration rate μ_{fe} is increased along with the increase of the thickness of the second a-Si layer. Therefore, when the thickness of the second a-Si layer is about 2000 angstroms, the TFT has the best electrical characteristics.

[0062] The present invention discloses controlling the flux ratio of H_2/SiH_4 to be within a range of from 0.40 to 1.00 to form the first a-Si layer having defects in the first embodiment, so as to reduce the photo leakage current I_{photo} of the element. Moreover, the present invention discloses modifying the film thickness of the second a-Si layer in the second embodiment, so that the best electrical characteristics can be obtained. Although the first and the second embodiment are disclosed respectively above, it does not mean they cannot work well together. In order to further improve the element characteristics, the present invention may combine the contents disclosed in the second embodiment together to make the first a-Si layer and the second a-Si layer in the channel layer.

[0063] In summary, the TFT manufacture method of the present invention has at least the following advantages: 1. When

the first a-Si layer is formed by using the LDR, the flux ratio of H_2/SiH_4 is controlled within a range from 0.40 to 1.00. Although the film quality of the formed first a-Si layer is worse than in the prior art (since it has more defects), the TFT electrical characteristics considered as a whole, such as the on current I_{on} , the off current I_{off} , the threshold voltage V_{th} , and the electronic migration rate μ_{fe} , perform better than in the prior art. 2. The present invention modifies the film quality of the first a-Si layer. Since there are more defects in the first a-Si layer, the photo leakage current generated when the element is irradiated can be efficiently reduced. 3. The present invention obtains the optimum electrical characteristics of the element by modifying the film thickness of the second a-Si layer to a range from 1000 angstroms to 2000 angstroms.

[0064] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.